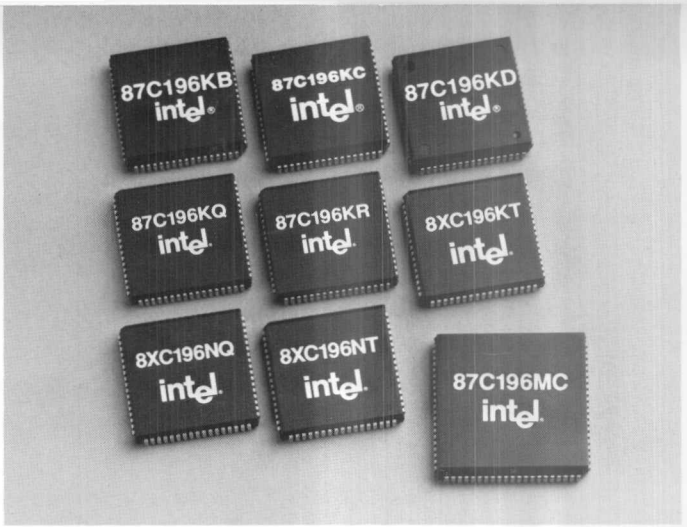
196 Microcontroller Family



Intel's broad portfolio of 196 microcontrollers has been designed to meet your varying peripheral, performance and memory size requirements.

Overview

Intel's 196 Microcontroller Product Family is the industry standard for 16-bit embedded microcontrollers. The 8XC196 products are found in a wide variety of embedded applications. The high-performance register to register architecture is well suited for complex real-time control applications such as hard disk drives, modems and motor control. Our broad portfolio of 8XC196 microcontroller products has been designed to meet your varying peripheral, memory size, addressability and performance requirements.

The 8XC196 family shares a common core architecture which is register based. The MCS®-96 register architecture eliminates the accumulator bottleneck and enables fast context switching. All devices have bit, byte, word and some 32-bit operations. The following table summarizes arithmetic performance at different clock frequencies:

OPERATION	12 MHz	16 MHz	20 MHz
16 + 16 ADD	0.66 us	0.50 us	0.40 us
16 x 16 MULTIPLY	2.3 us	1.75 us	1.4 us
32 by 16 DIVIDE	4.0 us	3.0 us	2.4 us

The 8XC196 Bus Controller features programmable waitstate generation, 8- or 16-bit buswidth, and features a HOLD/HLDA protocol for multiprocessor systems.

The newest member of the 8XC196 family, the 87C196NT, has extensions built into the core to support 1 MByte of linear address space, and features an enhanced bus controller that allows no waitstate operation with slower low-cost memories.

Products

The 8XC196KB, 8XC196KC, 8XC196KD family

8XC196KB

The 8XC196KB is the first member of the CHMOS* MCS-96 family. It is available in CPU only, 8K ROM, and 8K byte OTPROM versions. All versions feature 232 bytes of Register RAM.

The 8XC196KB uses the High-Speed Input/Output (HSIO) structure for event control. The HSIO has up to 4 input and 6 output lines, and uses either of two timer/counters as a time base. Additional features include a hardware-generated Pulse Width Modulator (PWM), a full-duplex Serial I/O (SIO) port, a watchdog timer and an 8-channel 10-bit resolution Analog to Digital (A/D) converter.

The 8XC196KB has 48 Input/Output (I/O) lines which are shared with the peripherals.

Reduced pin count devices are available for applications not requiring all the standard features.

8XC196KC

The 8XC196KC is the next step up in the CHMOS 196 family. It is available in CPU, 16K byte ROM and 16K byte OTPROM versions. All versions feature 488 bytes of Register RAM.

The 8XC196KC has all the same peripherals as the 8XC196KB, but adds the following features: There are now a total of three hardware PWM generators, the A/D converter has both 8- and 10-bit conversion modes with programmable sample and conversion times, and a Peripheral

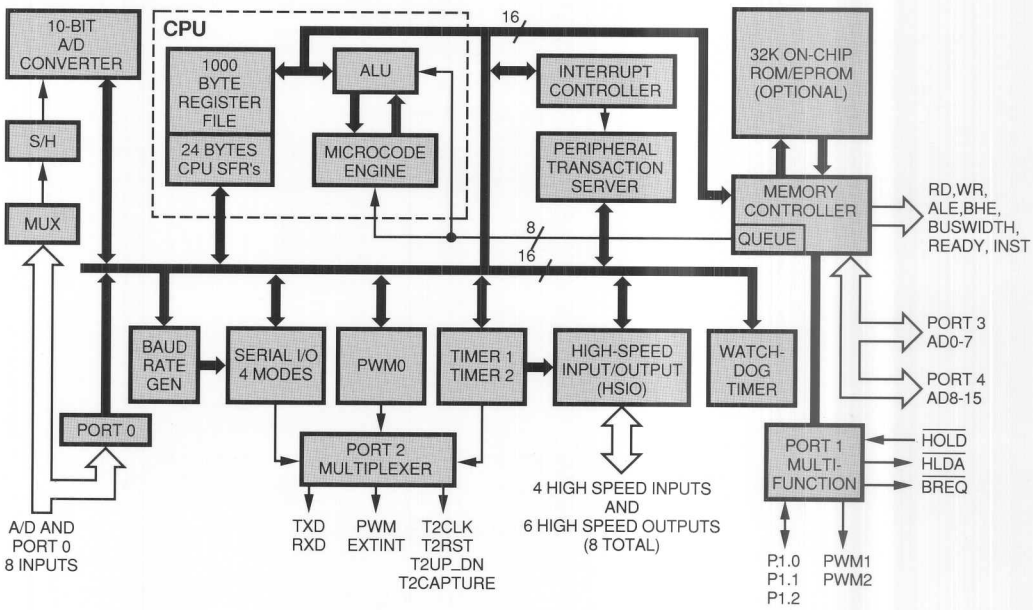
Transaction Server (PTS) has been added. The PTS acts as a microcoded interrupt handler which lessens CPU overhead during interrupt servicing.

8XC196KD

The 8XC196KD has all the features of the 8XC196KC, but has extended the on chip memory. The 8XC196KD is available in 32K byte ROM and 32K byte OTPROM versions. Both versions feature 1000 bytes of Register RAM. With the availability of 32K of memory, program development in high level languages becomes much more practical. The 8XC196KD is the first MCS-96 device to be offered in a 20 MHz version, allowing an immediate 25% increase in performance.

Key Features

- Up to 20 MHz Operation
- Fast Register to Register Architecture
- Up to 1000 Bytes Register RAM
- Up to 32K Internal EPROM
- Dynamically Configurable 8- or 16-Bit Buswidth
- HOLD/HLDA Bus Protocol
- 8-Channel High Speed I/O (HSIO) Subsystem
- 16-bit Timer
- 16-Bit Counter
- Up to 3 Dedicated PWM Generators
- Full Duplex Serial Port
- 16-Bit Watchdog Timer
- Eight Channel 8- or 10-Bit A/D Converter
- Five 8-Bit I/O Ports
- IDLE and POWERDOWN Modes
- Peripheral Transaction Server (PTS) on KC and KD



8XC196KD Block Diagram

The 8XC196KQ, 8XC196KR, 87C196KT family

8XC196KQ

The 8XC196KQ is a highly integrated, advanced member of the MCS-96 family. It is available in 12K byte ROM and 12K byte OTPROM versions. Both versions feature 360 bytes Register RAM, and an additional 128 bytes Internal RAM. The Internal RAM may be used for program execution or data storage.

The 8XC196KQ uses a new modular Event Processor Array (EPA) for event monitoring and control. The EPA has a 250 ns resolution at 16 MHz, and has 10 capture/compare modules plus two compare only modules. The EPA is extremely flexible, and has pulse-width modulation (PWM) generation ability.

The 8XC196KQ includes the Peripheral Transaction Server (PTS) introduced on the 8XC196KC, but has changed some of the modes to support PWM generation with the EPA.

The 8XC196KQ has a slave port which is used to interface to another system's bus. The slave port feature can be used to make the 8XC196KQ a versatile, programmable peripheral attached to any PC's bus.

There are two serial ports on the 8XC196KQ: one is the standard SIO module found on the 8XC196KB, and the other is a Synchronous Serial I/O (SSIO) port. The SSIO is capable of full duplex synchronous communication. Both SIO's have their own programmable baud rate generators.

The 8XC196KQ A/D converter is based on the 8XC196KC design, but has additional modes which allow programmable threshold detection and offset correction.

The 8XC196KQ has 56 I/O lines which are shared with the peripherals.

A reduced pin count version of the 8XC196KQ is available (8XC196JQ) for designs not requiring all the standard features.

8XC196KR

The 8XC196KR is a memory scalar version of the 8XC196KQ device. It retains all of the 8XC196KQ features, and is available in 16K byte ROM or 16K byte OTPROM versions. Both versions feature 488 bytes Register RAM and 256 bytes Internal RAM. A reduced pin count version is available (8XC196JR).

87C196KT

The 87C196KT is an enhanced version of the 8XC196KR and is available in 32K byte OTPROM version. This features 1000 bytes Register RAM, and 512 bytes Internal RAM. Additionally, the 87C196KT's bus controller has new modes which allow no waitstate operation with slower external memory.

Key Features

- Up to 16 MHz Operation
- Fast Register to Register Architecture
- Up to 1000 Bytes Register RAM
- Up to 512 Bytes Internal RAM
- Up to 32K Internal EPROM
- Dynamically Configurable 8- or 16-Bit Buswidth
- HOLD/HLDA Bus Protocol
- Ten Channel Event Processor Array (EPA)
- Two 16-bit Timer/Counters with Prescaler and Quadrature Counting Mode

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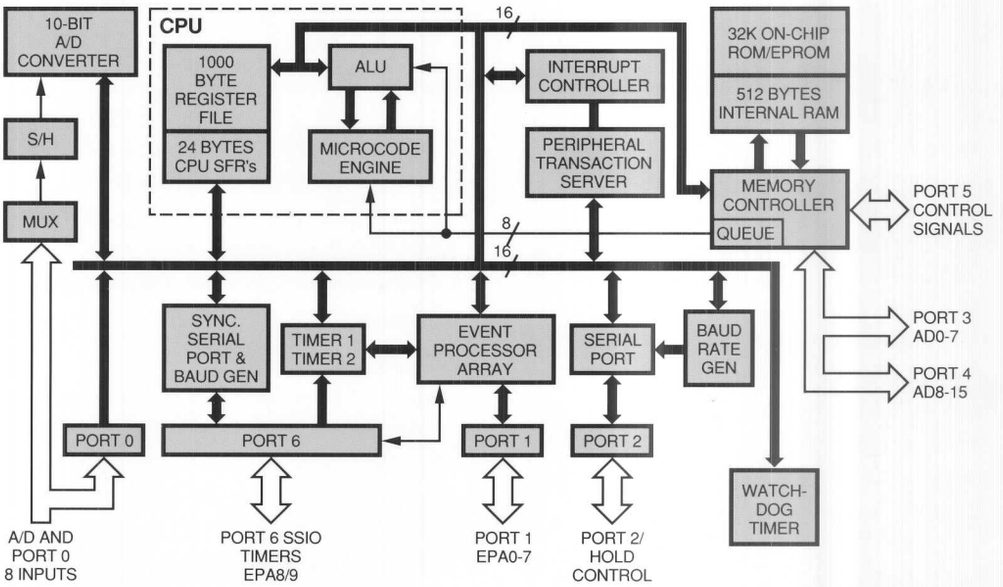


87C196KT Block Diagram

- Full Duplex Serial Port with Independant Baud Rate Generator
- Full Duplex Synchronous Serial Port (SSIO)
- Slave Port For Direct Interprocessor Communication
- 16-Bit Watchdog Timer
- Eight Channel 8- or 10-Bit A/D Converter
- Six 8-Bit I/O Ports
- IDLE and POWERDOWN Modes
- Peripheral Transaction Server (PTS)
- Enhanced Bus Modes on KT

The 87C196NQ, 87C196NT family

The 87C196NQ and 87C196NT are the first members of the MCS-96 family to offer addressability beyond 64K bytes. Both these devices have extensions to the core architecture which support 20 address lines for a 1 Mbyte linear address space. Nine new instructions have been added which support extended addressing. Additionally, an enhanced bus controller allows no waitstate operation with slower memories.

87C196NQ

The 87C196NQ is a highly integrated and advanced member of the MCS-96 family. It is available in 12K byte OTPROM version. This version features 360 bytes Register RAM, and an additional 128 bytes Internal RAM. The Internal RAM may be used for program execution or data storage.

The 87C196NQ uses the Event Processor Array (EPA) for event monitoring and control. The EPA has a 250 ns resolution at 16 MHz, and has 10 capture/compare modules plus two compare only modules. The EPA is extremely flexible, and has PWM generation ability.

The 87C196NQ includes the same Peripheral Transaction Server (PTS) introduced on the 8XC196KQ.

The 87C196NQ has a slave port which is used to interface to another system's bus. The slave port feature can be used to make the 87C196NQ a versatile, programmable peripheral attached to any PC's bus.

The 87C196NQ has the same two serial ports that are found on the 8XC196KQ. One is the standard SIO module found on the 8XC196KB, and the other is a Synchronous Serial I/O (SSIO) port. The SSIO is capable of full duplex synchronous communication. Both SIO's have their own programmable baud rate generators.

The 87C196NQ A/D converter is based on the 8XC196KQ design, but has only 4 A/D inputs.

The 87C196NQ has 56 I/O lines which are shared with the peripherals.

87C196NT

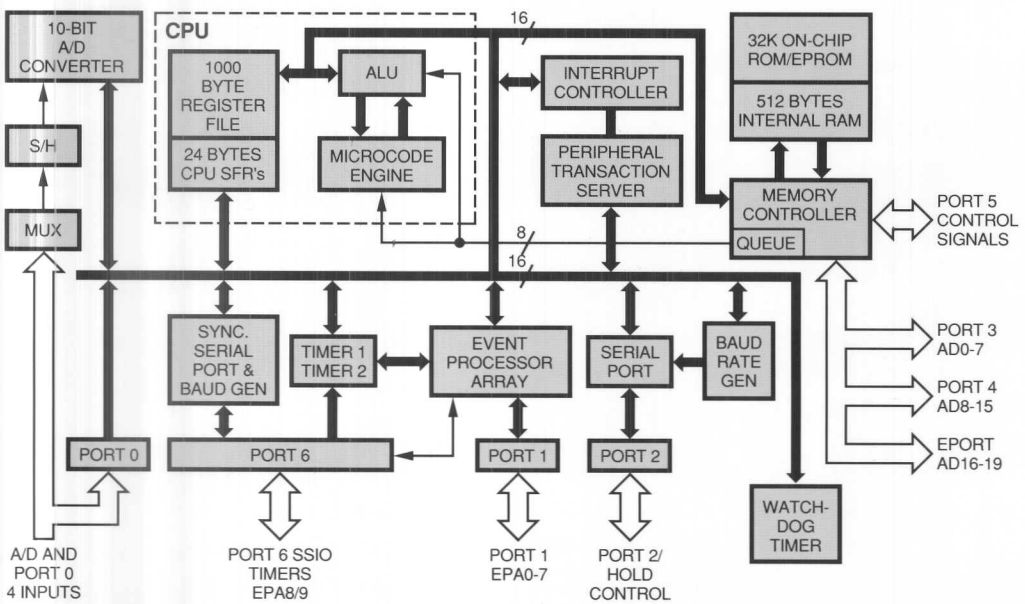
The 87C196NT is a memory scalar version of the 87C196NQ, and is available in 32K byte OTPROM version. This version features 1000 bytes Register RAM, and 512 bytes Internal RAM.

Key Features

- Mbyte Linear Address Space
- Up to 16 MHz Operation
- Fast Register to Register Architecture
- Up to 1000 Bytes Register RAM
- Up to 512 Bytes Internal RAM
- Up to 32K Internal EPROM
- Dynamically Configurable 8- or 16-Bit Buswidth
- HOLD/HLDA Bus Protocol
- Ten Channel Event Processor Array (EPA)
- Two 16-bit Timer/Counters with Prescaler and Quadrature Counting Mode
- Full Duplex Serial Port with Independant Baud Rate Generator
- Full Duplex Synchronous Serial Port (SSIO)
- Slave Port For Direct Interprocessor Communication
- 16-Bit Watchdog Timer
- Four Channel 8- or 10-Bit A/D Converter
- Six 8-Bit I/O Ports
- IDLE and POWERDOWN Modes
- Peripheral Transaction Server (PTS)
- Enhanced Bus Modes

The 8XC196MC

The 8XC196MC is the first member of the MCS-96 motor control family. This



87C196NT Block Diagram

device has peripherals which are optimized for three-phase AC induction motor control and power inverter applications. The 8XC196MC is available in 16K byte ROM and 16K byte OTPROM versions. Both versions feature 488 bytes Register RAM.

The 8XC196MC has a unique peripheral, the Waveform Generator (WFG) which is used to generate a three-phase pulse-width modulation (PWM). The WFG generates three complementary non-overlapping PWM pulses with resolutions of 125 ns (edge trigger) or 250 ns (centered). The WFG features programmable frequency, duty cycle and dead times. The WFG has two programmable high drive capability outputs for each phase. The outputs have programmable polarity, or may be forced high or low. A protection circuit allows disabling of all outputs simultaneously in response to an external event.

The 8XC196MC has two hardware PWM generators. These have a common programmable frequency, and separately programmable duty cycles.

The 8XC196MC uses the Event Processor Array (EPA) for event monitoring and control. There are 6 capture/ compare modules, and 6 compare only modules. The EPA features 125 ns time resolution.

The 8XC196MC A/D converter is a 13 channel version of the 8XC196KQ's. It operates in 8- or 10-bit mode, and has programmable sample and convert times, threshold detect mode and offset correction.

A Peripheral Transaction Server (PTS) supports microcoded interrupt processing requiring less CPU intervention. A special PTS mode supports the Serial I/O (SIO) function.

The 8XC196MC has a total of 53 I/O lines which are shared with the peripherals. Reduced pin-count packages are available for applications not requiring all the standard features.

Key Features

- Three Phase PWM Waveform Generator
- Up to 16 MHz Operation
- Fast Register to Register Architecture
- Bytes Register RAM
- 16K Internal EPROM
- Dynamically Configurable 8- or 16-Bit Buswidth
- HOLD/HLDA Bus Protocol
- Eight Channel Event Processor Array (EPA)
- Two 16-bit Timer/Counters with Prescaler and Quadrature Counting Mode
- 16-Bit Watchdog Timer
- Channel 8- or 10-Bit A/D Converter
- Six 8-Bit I/O Ports
- IDLE and POWERDOWN Modes
- Peripheral Transaction Server (PTS)

Development Tool Support

Software Development

Intel provides a complete software development package for the 8XC196 Family. It includes:

- ASM-96
- 32-Bit Floating Point Library
- RL-96 Linker/Relocater
- iC-96
- PLM-96
- Object-to HEX code converter

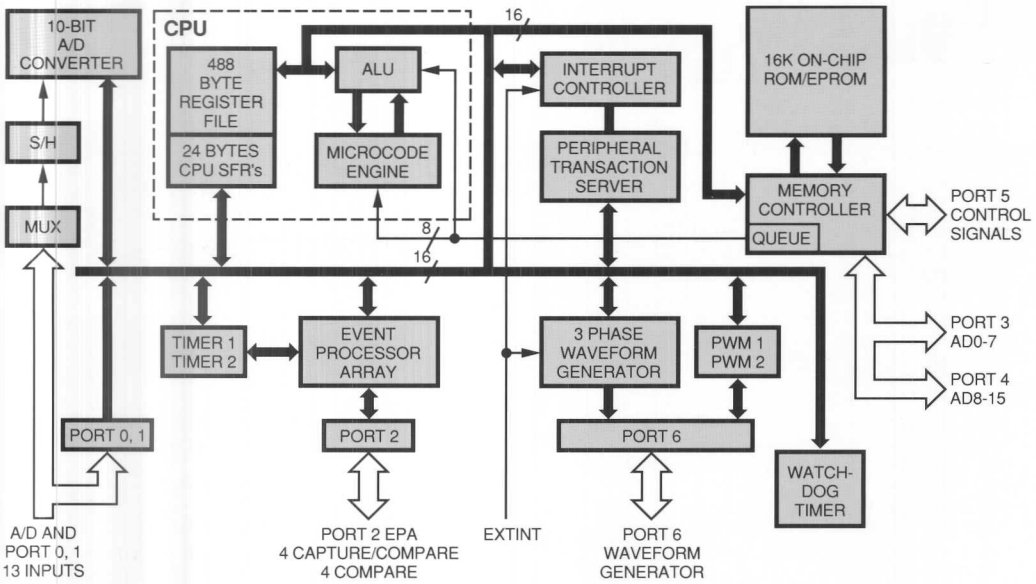
In-Circuit Emulation

Complete solution for the 8XC196KB/ KC/KD microcontrollers. Intel ICE products provide:

- Windowed human interface
- Pull-down menus
- On-line help

Evaluation Boards

The EV80C196Kx family of evaluation board products are available to assist you in software development and debugging.



8XC196MC Block Diagram

	ROM / EPROM	REGISTER RAM	INTERNAL (CODE) RAM	TIMER / COUNTERS	ANALOG INPUT CHANNELS	I/O PINS	I/O TYPE	SERIAL PORTS	SPEED (MHz)	PROCESS	PACKAGE	ONCE TEST MODE	TOOLS	ADDRESS SPACE	KEY FEATURES
8XC196KB/ 8XC196KB16	8K	232	NO	2	8	48	HSIO	1	10, 12, 16	CMOS	N, S, U	YES	A, B, C, E, I, P	64K	Low-Power, High Performance CMOS
8XC194/ 8XC196	8K	232	NO	2	0, 4	48	HSIO	1	16	CMOS	N, S	YES	A, B, C, E, I, P	64K	Lower-Cost, 8-Bit Bus, 0 or 4 Channel Version of KB
8XC196KC	16K	488	NO	2	8	48	HSIO	1	16	CMOS	N, S	YES	A, B, C, E, H, I, P	64K	16K EPROM, 488 Byte RAM 3-PWM, PTS
8XC196KD/ 8XC196KD20	32K	1000	NO	2	8	48	HSIO	1	16, 20	CMOS	N, S	YES	A, B, C, D E, H, I, P	64K	32K EPROM, 1000-Byte RAM Version of KC
8XC196JQ	12K	360	128	2	8	41	6 EPA	2	16	CMOS	N-52	YES	I, A, C, P, E	64K	6 EPA, 6 A/D 52-Lead Package for Cost Sensitive Applications
8XC196JR	16K	488	256	2	8	41	6 EPA	2	16	CMOS	N-52	YES	I, A, C, P, E	64K	6 EPA, 6 A/D 52-Lead Package More Memory than JQ
8XC196KQ	12K	360	128	2	8	56	10 EPA	2	16	CMOS	N-68	YES	I, A, C, P, E	64K	10 EPA, 8 A/D, 56 I/O lines
8XC196KR	16K	488	256	2	8	56	10 EPA	2	16	CMOS	N-68	YES	I, A, C, P, E	64K	Memory Scaler Version of KQ
87C196KT	32K	1000	512	2	8	56	10 EPA	2	16	CMOS	N-68	YES	I, A, C, P, E	64K	Memory Scaler version of KR with Enhanced Bus Controller
87C196NQ	12K	360	128	2	8	56	10 EPA	2	16	CMOS	N-68	YES	I, A, C, E	1 M	1 Mbyte Linear Address Range Enhanced Bus Controller
87C196NT	32K	1000	512	2	4	56	10 EPA	2	16	CMOS	N-68	YES	I, A, C, E	1 M	1 Mbyte Linear Address Range Memory Scaler Version of NQ